REMARKS

This paper is responsive to the Non-Final Office Action dated August 12, 2005. Claims 1-58 are pending.

Information Disclosure Statements

Applicant filed an IDS on July 9, 2004, and an initialed copy of the Form PTO-1449 was returned in the previous Office action. However, one of the references was not initialed by the examiner. Applicant respectfully requests the Examiner to initial reference number AM and return another copy of Form PTO-1449 with the next Office action.

Drawings

The Office action does not indicate whether the drawings filed on September 17, 2003 are acceptable. Applicant respectfully requests the Examiner to so indicate in the next Office action.

Claim Objections

Applicant has amended claim 44 to delete the word "sensing" as requested by the Examiner.

Claim Rejections - 35 U.S.C. § 102

Claims 1-8, 10-11, 13-22, 24-30, 32, 34-43, 45-48 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Komarek et al. (U.S. Patent No. 5,650,979). Applicant respectfully traverses this rejection.

Regarding claim 24, the Examiner has cited Komarek et al. in Fig. 10 and at column 27, lines 14-16 in support of the assertion that Komarek et al. discloses a circuit comprising "first and second matched devices which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices, said shift giving rise to a mismatch in the characteristic between the matched devices."

Applicant respectfully submits that the cited text (column 27, lines 14-16) describes a sensing stage 300 which is used to detect the difference between the two dummy bit lines DMYON and DMYOFF as used and described in connection with the sense amplifier of Fig. 12 (see column 26, lines 58-61) and also in connection with the sense amplifier of Fig. 10. The cited text states that the sensing stage 300 is designed to match the characteristics of the sense amplifier. Nowhere does Komarek et al. teach that such matched devices are susceptible to an *accumulated data-dependent* post-manufacture *shift* in a characteristic of one or more of the matched devices.

The Examiner has also cited Komarek et al. at column 11, lines 54-63 in support of the assertion that Komarek et al. discloses a preconditioning circuit for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device. This cited text recites:

> The improvement further comprises an amplifier circuit having its input coupled to the output of the sensing stage circuit and having an output for generating the amplified difference of the voltage on the first and second dummy word lines. A level detect circuit has an input coupled to the output of the amplifier circuit. The level detect circuit converts the output of the amplifier circuit to a preconditioned signal. An inhibit circuit prevents false triggering during a nonsensing time period when a predetermined precharge signal is active. (column 11, lines 54-63)

Applicant respectfully suggests that the Examiner has confused a "preconditioned signal" generated by the level detect circuit described in this cited text with the cited limitation in the claim. Stated more precisely, this passage does not teach or suggest a "*preconditioning circuit* for subjecting the matched devices to a particular condition for a length of time sufficient to *cause an initial shift* in the characteristic in each of the matched devices and *to thereby reduce* an expected magnitude of *any further lifetime shift* in the characteristic of either matched device" as recited in the claim.

The Examiner has also cited Komarek et al. at column 2, lines 10-13 in support of this same assertion. This cited text recites:

> For example, in the circuit of FIG. 16, the threshold value of the initial input inverter 10 is inevitably shifted by the high transconductance of the driving transistor to cancel out the hysteresis property normally provided by load transistor 14 as described above. (column 2, lines 9-13)

This passage describes an input buffer, and specifically describes the shifting of the initial input inverter 10 threshold value in response to noise induced by, for example, output buffer switching (see column 2 at lines 2-9). Such a shift in the threshold *of the inverter circuit* is transient and only occurs during the noise disturbance. Moreover, this shift occurs even though the threshold voltage *of the individual transistors* does not vary. In addition, there are not even any matched devices described in this circuit. As such, this passage provides no teaching whatsoever of any "*preconditioning circuit* for subjecting the matched devices to a particular condition for a length of time sufficient to *cause an initial shift* in the characteristic in each of the matched devices and *to thereby reduce* an expected magnitude of *any further lifetime shift* in the characteristic of either matched device" as recited in the claim.

In addition, the Examiner has also cited Komarek et al. at column 17, lines 14-41 in support of this same assertion. This passage, too, describes an input buffer circuit having a hysteresis effect. In this passage, as before, the use of the term "threshold voltage" in describing VT1 and VT2 is clearly used to describe *buffer* threshold voltages, not individual device threshold voltages. The shifting of the "threshold voltage" in this passage is clearly taught as being controlled by which transistors are turned on at any given point in time. For example, this passage in part recites:

> The threshold voltage VT2 as set by inverter 50, and transistors 52 and 53, is lower than the threshold voltage VT1 which is determined by inverter 50 alone since the driving force to inverter node 48 is increased by transistors 52 and 53. (column 17 lines 26-30)

Again Applicant asserts that this passage provides no such teaching as alleged by the Examiner.

In addition, Applicant respectfully traverses several of the positions advanced by the Examiner regarding subject matter allegedly disclosed by Komarek et al. that is relevant to certain of the dependent claims. For example, the Examiner cites Figure 10 as disclosing first

and second matched devices that together comprise a cross-coupled pair of transistors within a sensing circuit of a semiconductor memory. Applicant respectfully submits that there are no such cross-coupled transistors within Fig. 10.

Moreover, the Examiner cites the VBIAS node in Figure 10 as being a preconditioning circuit which comprises means for applying a substantially uniform bias history across both the first and second matched devices. Applicant respectfully submits that there is no such circuitry shown anywhere in Fig. 10 that can function in a manner as recited in the claim limitation. Indeed, the P-channel load devices, being arranged in a traditional current mirror configuration, virtually ensures that the bias across the left most P-channel load device remains different than the bias across the right-most P-channel load device, irrespective of the data polarity sensed by such a circuit.

The Examiner cites the B waveform shown in Figure 15 as illustrating a predetermined bias condition (which is subjected to each of the matched devices) which includes a negative gate-to-source voltage. The transistor having a negative gate-to-source voltage which this figure describes is transistor 216 in Fig. 14. This device does not correspond to one of the matched devices as claimed. It is just a random transistor somewhere in the circuit (and unrelated to any matched device) that the Examiner has identified as having, for an unspecified amount of time, a negative gate-to-source voltage.

Regarding the method claims 1-23, the Examiner has advanced the position that the apparatus disclosed by Komarek et al. *would* perform the claimed method. Applicant respectfully submits that Komarek et al. nowhere describes performing such a preconditioning step, nor does Komarek et al. describe any circuit even capable of performing such a preconditioning step as recited in the claims. Even assuming, *arguendo*, that the alleged circuitry *could* perform such a preconditioning step as recited in the various claims, there nonetheless is no teaching or suggestion of doing so. Moreover, no such operation is believed to be inherent in any disclosed circuitry.

With all due respect, Applicant believes that the Komarek et al. reference is utterly mis-applied to the claims of the instant application, and requests the Examiner to withdraw the rejection. There is no teaching or even suggestion of <u>any</u> of the claims at issue.

PATENT

Claims not addressed by this Office action

Applicant calls the Examiner's attention to a believed error in the Office action. There are 58 claims pending in the instant application, being claims 1-58. However, the Office Action Summary does not indicate the status of claims 49-58, nor does the Detailed Action indicate the status of, or discuss in any way, claims 49-58. Applicant believes that a prima facie case has not been made out for the rejection of claims 49-58, since no basis for such a rejection has been provided. Applicant respectfully requests the Examiner to indicate the status of these claims on the next Office action.

Allowable Subject Matter

Claims 9, 12, 23, 31, 33, and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In light of the believed allowability of the remaining claims, these claims remain without amendment.

Summary

Claims 1-58 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Andrew C. Graham — Date: 10-18-05

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